TECHNotes

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Unlocking the Layers: A Metallographic Exploration of Integrated Circuits (ICs)

In the fast-paced world of modern technology, integrated circuits (ICs) are the backbone of almost every electronic device we use. From smartphones to aerospace systems, ICs drive the functionality of today's devices. But how do we ensure these tiny, yet complex components meet the rigorous standards of performance and reliability required in critical applications? This is where **metallographic delayering** becomes essential—a technique that allows engineers to dive deep into each layer of these sophisticated microchips.

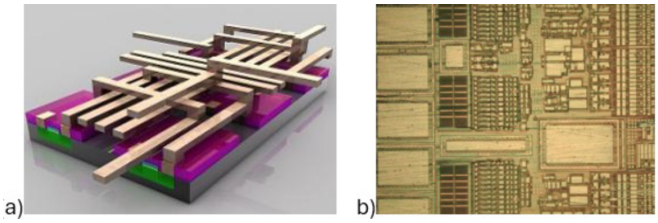


***Figure 1**. (a) 3D representation of an IC showing metal interconnects (b) interconnection within a chip*

Metallographic delayering is a crucial analytical tool used to progressively remove the layers of an IC, providing a detailed view of its structural integrity, design, and potential weaknesses. In this article, we explore the purpose, methodology, and applications of IC delayering, emphasizing its role in **failure analysis** and **reverse engineering**.

What Is Metallographic Delayering?

Metallographic delayering involves the sequential removal of layers from an integrated circuit to reveal its internal structure. This technique enables engineers to inspect each layer of the IC, from the top passivation layer down to the silicon substrate, to investigate issues, verify designs, and ensure functionality.

Unlike traditional cross-sectional analysis, which offers a static side view of the IC, delayering provides a sequential examination of each layer, uncovering components such as **metal interconnects, vias,** and **transistor gates**. This level of detail is crucial for understanding the microstructure of ICs, making delayering indispensable in high-reliability sectors.

Why Metallographic Delayering of ICs Matters?

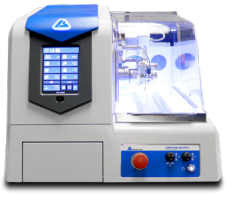
Consider a scenario where a critical aerospace system malfunctions due to an undetected defect in an integrated circuit. Understanding the root cause of such failures is vital to prevent future issues, and this is where metallographic delayering plays a crucial role. Ensuring the quality, reliability, and functionality of integrated circuits is essential in the competitive electronics industry. Metallographic delayering plays a key role in:

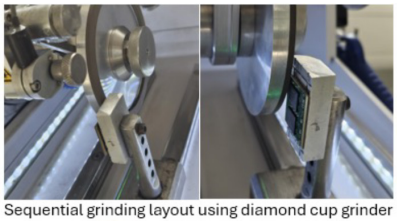
1. **Failure Analysis** - When an IC fails, understanding the root cause is crucial for preventing future failures. Delayering allows analysts to systematically peel back each layer of the IC and locate defects, such as **cracked vias, short circuits,** or **electromigration** issues within metal traces. This process is especially important for applications in **aerospace** and **automotive electronics**, where failures can have severe consequences.
2. **Reverse Engineering** - Delayering is also invaluable for **reverse engineering**. By analysing each layer in detail, engineers can determine the design and layout of an IC, gaining insights into a competitor's product or verifying the authenticity of a purchased chip. This helps ensure compliance and identify potential infringements of **intellectual property (IP)**.
3. **Quality Control** - Delayering helps ensure that ICs are fabricated according to design specifications. Through a detailed, layer-by-layer inspection, manufacturers can verify that the **fabrication process** has produced consistent and defect-free structures. This level of quality control is critical for high-reliability sectors, such as **medical devices** and **military applications**.

How IC Delayering Works: The Process

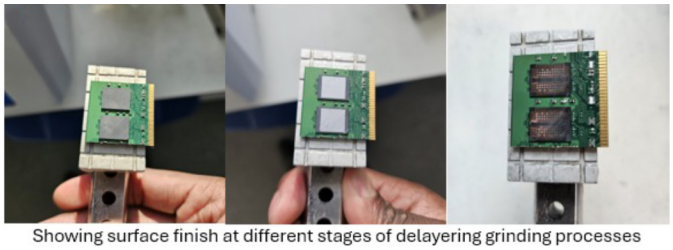
The delayering of ICs involves a series of meticulously controlled steps, organized in a logical sequence for clarity:

- **Sample Sectioning and Grinding**: The IC sample is sectioned off a PCBA and secured onto a wafer chuck using high temperature wax (crystal bond). The sample is then sequentially ground at increments of 5-20microns depending on an ICs chip encapsulation material and layer thicknesses. Once close to layer of interest, the test sample is then taken to grinding and polishing steps using finer abrasives on an EcoMet 30 polishing machine.





Sequential grinding layout using diamond cup grinder



Showing surface finish at different stages of delayering grinding processes

***Figure 2**. Showing Mechanical delayering of an IC*

- **Sample mounting**: The IC sample can be embedded in **epoxy resin** to provide mechanical support and protect delicate structures during grinding and polishing. Alternatively, as shown above, the IC can be secured using Crystal bond wax for subsequent stages

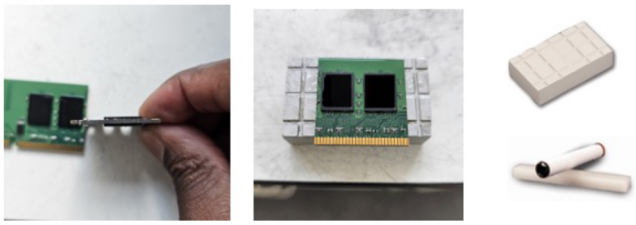


Figure 2. IC after sectioning and mounting on a wafer chuck

- **Mechanical Grinding and Polishing**: The IC surface is mechanically ground and polished using progressively finer abrasives to expose each layer without causing damage. Ensuring planar surface is a challenge but can be optimised by using fixed diamond grinding surfaces such as UltraPrep films or FiberMet film discs that have embedded diamond abrasive particles ranging from 30micron to 1micron.

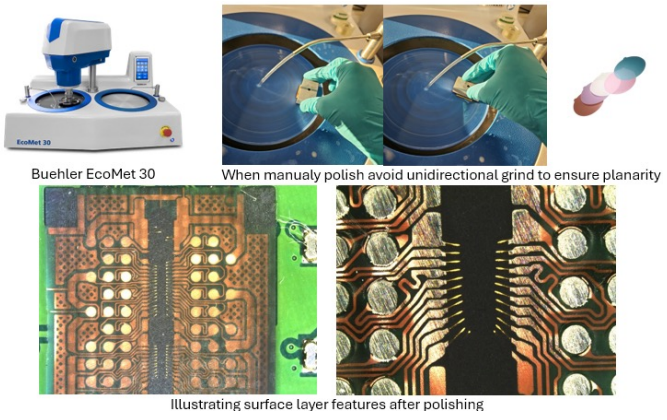


Figure 3. Images illustrating delaying at the BGA to PCB board layers

- **Chemical or Plasma Etching**: Depending on the material, **chemical etching** or **plasma etching** can also be adopted to selectively remove specific layers, preserving features for subsequent imaging.
- **Sequential Delayering**: The process is repeated layer by layer until the entire IC has been analysed, revealing defects, design issues, or inconsistencies.
- **Microscopy and Analysis**: After each layer is exposed, **optical microscopy** or **SEM** is used to capture high-resolution images and inspect components such as **metal traces, vias**, and **transistors**.

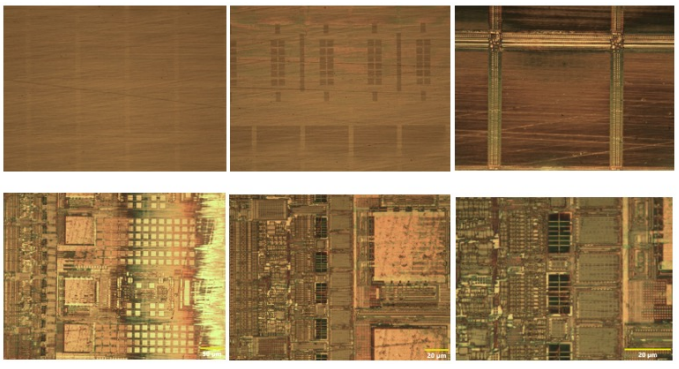


Figure 4. illustrating ICs pattern microstructure of different layers as observed starting from the last pattern applied on a silicon die.

Applications of Metallographic Delayering

Metallographic delayering plays a critical role in ensuring the reliability, performance, and security of electronic components across different industries. By examining each layer in detail, delayering helps address key challenges and provides solutions that directly impact the quality of products used in aerospace, automotive, and consumer electronics.

Here are some notable applications of metallographic delayering:

1. **Detecting Manufacturing Defects -** Delayering can be used to detect **manufacturing defects**, such as **misaligned vias**, **metal voids**, or **delaminations**, that could lead to reliability issues. Early detection of these defects helps manufacturers implement corrective actions before components reach end-users, reducing warranty claims and product failures.
2. **Intellectual Property Protection** - Delayering is also used for **IP protection** by verifying whether a competitor's IC design infringes on patented technology. By analyzing and comparing the internal architecture of two ICs, manufacturers can determine whether their proprietary designs have been copied.
3. **Research and Development (R&D)** - In **R&D**, delayering helps engineers understand the effectiveness of different materials and design approaches. For example, analyzing the performance of various **dielectric materials** or **interconnect designs** can lead to improved IC performance, reduced power consumption, or enhanced reliability.

Key Challenges in IC Delayering

Metallographic delayering, while extremely powerful, presents several challenges:

- **Precision**: The process requires extreme precision to ensure that each layer is removed uniformly without damaging the underlying structures. This is particularly challenging with modern ICs that have **nanometer-scale features**. For instance, in high-density ICs, even slight over-polishing can damage critical interconnects, leading to inaccurate analysis results. Techniques such as using X-ray CT scanners can aid in the analysis but cost and resolution capability are key considerations here.
- **Material Variability**: ICs are made up of different materials, such as **copper, silicon dioxide**, and **polysilicon**, each with different hardness and chemical properties. This requires careful selection of grinding, polishing, and etching techniques to handle each layer appropriately.
- **Analysis Complexity**: Modern ICs are densely packed, with multiple layers of metal interconnects and transistors. Analysing the intricate features of each layer requires advanced microscopy techniques and significant expertise.

Quality Control Standards for IC Delayering

To ensure that metallographic delayering is conducted in a manner that yields accurate and reliable data, the following quality control standards are often applied:

- **JEDEC Standards**: The **JEDEC** organization provides standards for microelectronics, including guidelines on evaluating semiconductor reliability and performing **failure analysis**.
- **IPC Standards**: **IPC-9012** provides guidelines for microsectioning and metallographic procedures, which are highly relevant to IC delayering. These standards ensure that the delayering process is performed consistently and yields reliable data for analysis.
- **ASTM Standards**: The **ASTM E3** standard covers the preparation of metallographic specimens and ensures that IC samples are properly prepared for delayering without introducing artifacts that could impact analysis.

Conclusion: Delayering as a Critical Tool for IC Reliability

Metallographic delayering of ICs provides invaluable insights into the internal architecture of electronic components. Whether it is for **failure analysis, reverse engineering**, or **quality control**, delayering is an indispensable tool for understanding what lies beneath the surface of an IC. By meticulously removing and analysing each layer, engineers can detect manufacturing defects, verify design specifications, and enhance the reliability of electronic components used in mission-critical applications.

As the **electronics industry** continues to push the boundaries of miniaturization and complexity, the role of metallographic techniques like delayering becomes even more critical. By leveraging these methods, manufacturers can continue to innovate and ensure that the electronic devices we rely on every day are robust, reliable, and ready for the future.

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